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Dr. Paolo Gargini is the Director of Technology Strategy for Intel Corporation. Dr. Gargini is also responsible for world-wide research activities conducted outside Intel for the Technology and Manufacturing Group by consortia, institutes and universities.

Dr. Gargini was born in Florence, Italy and received a doctorate in Electrical Engineering in 1970 and a doctorate in Physics in 1975 from the Università di Bologna, Italy, both with full honor and marks.

He has done research at LAMEL in Bologna, Stanford Electronics Laboratory, and Fairchild Camera and Instrument Research and Development in Palo Alto from 1970 to 1977. Since joining Intel in 1978, Dr. Gargini has conducted studies on Process Reliability; he was responsible for developing the building blocks of HMOS III and CHMOS III technologies used in the 1980's for the 80286 and the 80386 processors. In 1985 he headed the first submicron process development team at Intel.

Dr. Gargini has been the Chairman of the Executive Steering Council (ESC) of I3001 and, subsequently, of International Sematech from 1996 to 2000. He is now a member of the Sematech Board. Since 1998, Dr. Gargini has been the Chairman of the International Technology Roadmap for Semiconductors (ITRS).

He is a member of various technical committees and technical advisory boards for organizations such as the Semiconductor Research Corporation (SRC), and the Technology Strategic Council (TSC) of the SIA in the US, IMEC in Europe, ASET and MIRAI in Japan.

He also heads the International EUV Initiative (IEUVI), formed in 2001, that fosters cooperation and coordination among the largest EUV consortia in the world.

Dr. Gargini is the facilitator of the International Consortia Cooperation Initiative (ICCI). This initiative, started in 2000, fosters exchange of information among a selected group of leading consortia and institutes in the world.

In September 2003, Dr. Gargini was included by EE Times in a very selected group of Influencers of the semiconductor industry with the following motivation: "EE Times has chosen 13 people who are influencing the course of semiconductor development technology and taking it into realms that exceed the bounds set by the inventors of the transistor more than 50 years ago. With more than 25 years in the industry, Gargini is helping to navigate tough process and manufacturing waters."

Dr. Gargini initiated and became the first Chairman of the Governing Council of the Nano Electronics Research Initiative (NERC) funded in June 2005 by SIA. This Initiative is aimed at supporting and focusing research in universities towards subsequent commercialization of Nanoelectronics. NERC actively cooperates in this effort with USG organizations such as NNI, NSF, DARPA, and NIST.

Dr. Gargini was elevated to IEEE Fellow in 2008.

Dr. Gargini was elevated to IEC Fellow in 2009.