

## **SEMICO IMPACT CONFERENCE SERIES**

### **Semico Impact June 2005 Post Event Recap**

The Semiconductor IP event in this series was held June 9, 2005 at the San Jose Wyndham Hotel.

*This recap is not meant to be all inclusive, but rather a brief snapshot of the exciting dialog that took place over the course of the conference.*

## **EMBEDDED MEMORY PANEL: How Dense Can We Go and Why Should We?**

Moderator: Bob Merritt, VP of Emerging Markets, Semico Research Corp.

### **Mark-Eric Jones**

**President & CEO, Innovative Silicon**

[www.z-ram.com](http://www.z-ram.com)

Innovative Silicon is an IP business model company set up to exploit a patented technology representing a breakthrough in density for embedded DRAM. Mark-Eric Jones, President & CEO of Innovative Silicon said, "We see that the considerable user advantage is going to drive the demand for our Z-RAM memory technology." SOI has been an exciting way of making chips but it is expensive. However, by taking advantage of Z-RAM on SOI you can reverse the economics for most chips. Mr. Jones said, "In the past the main driver for embedding memory was to increase performance, and today the main driver is to reduce power consumption. The biggest challenge we have today is to find out how to achieve these advantages without breaking the bank." I/O power saving is today an important factor in choosing between SoC (System-on-Chip), SIP (Semiconductor Intellectual Property), or SoB (System on Board). The main difference between the three is the number of energy units per access. "The demand for memory is constantly increasing and power saving is possible by embedding; however, the cost of the die area is painful thereby driving innovation to find improved solutions—such as Z-RAM," concluded Mr. Jones. **(Approved by Speaker)**

### **Rakesh Sethi, Ph.D.**

**Director of Business Development, Toshiba America Electronic Components, Inc.**

[www.toshiba.com](http://www.toshiba.com)

Dr. Sethi agreed with Semico's statement that semiconductor IP is the next killer catalyst for semiconductor growth. "We are seeing that the IP market is going to be the driver for the next two nodes," said Dr. Sethi. "Toshiba has been able to keep up with our aggressive approach to advanced process technologies at 90nm; plus migration to 65, 45 and 32nm. The first thing we worry about is scalability in manufacturing," commented Dr. Sethi. The control of variation in processes is what makes or breaks your company. Toshiba announces product achievements after they are already shipping large quantities. This is contrary to the strategy of most of their competition. "At every node, we have a strategy to expand density through holistic design/packaging technology that will be coming on in the next two nodes for low cost," concluded Dr. Sethi. **(Approved by Speaker)**

### **Krishna Balachandran**

**Senior Director of Channel Marketing, Virage Logic**

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"Let me give you a different perspective on embedded memory," said Mr. Balachandran. "We heard Bob Merritt of Semico state earlier that real men have fabs but I'm going to say real men have/use embedded memory." The foundation of Virage Logic is built upon high-density products and application-optimized IP. Consumer applications are driving the need for embedded memory. "I am going to take the position that all real men need embedded memory but all men will use SRAM," stated Mr. Balachandran. "For example, we have a customer who has 2000 small SRAM memories on a chip and I know designers are not going to change it to have one big embedded DRAM—which means you need a multiple memories." So what are factors affecting the memory choice? He cited design architecture and cost being two key factors. Other factors include availability of advanced process geometries, reliability and working silicon. He stressed the need to know what IP is available, for what cost and at what process geometry. He pointed toward other factors affecting silicon cost such as; design time, silicon (area), mask/wafer, test escapes, yield/reliability and time-to-volume. "These factors play out before, during and after design so you need to go through the process in order to know which embedded memory will be most efficient," added Mr. Balachandran. "We need to synch physical IP with infrastructure IP in order to optimize yield, quality and shorter time-to-volume. If the physical IP and your test, diagnostics and repair are being done by separate parties you are going to run into test escapes, poor yield and unpredictable time-to-volume." "We believe that the Silicon Aware 6T SRAM is the workhorse memory IP for the foreseeable future," concluded Mr. Balachandran. **(Approved by Speaker)**

## **POWER MANAGEMENT PANEL: Power Requirements Continue to Climb, What Can Be Done?**

Moderator: Rich Wawryzniak, Senior Analyst, ASIC/SoC, Semico Research Corp.

**Arthur Swift**  
CEO, Transmeta

[www.transmeta.com](http://www.transmeta.com)

"Transmeta led the industry with a focus on energy efficient x86-compatible processing and we looked at things differently and innovated" said Mr. Swift. Over the last 2 years Transmeta has continued this legacy and transformed its business model from delivering its technologies only through its microprocessor products, to also deploy its technologies through IP licensing and synergistic engineering services. Some of these innovative technologies that Transmeta offers effectively address one of today's primary industry challenges: the rapid increase in power consumption. Collectively, these technologies are known as Transmeta's LongRun2. He noted, "You can apply it today, it can be retrofitted to existing bulk silicon designs and this solution can be complementary to other techniques." It has already been licensed to NEC, Fujitsu and Sony. "This power management approach delivers a practical solution for semiconductor scaling into the future," concluded Mr. Swift.

*(Approved by Speaker)*

**Mike McAweeney**  
Vice President, Industry Alliances, Cadence Design Systems, Inc.

[www.cadence.com](http://www.cadence.com)

"We are a design automation software company for the electronics supply chain," said Mr. McAweeney. He referenced the players of the silicon design chain; ARM, Applied Materials, TSMC, Artisan (now ARM's Physical IP) and of course, Cadence. "The motivation for power management comes from end market demands (convergence and mobility) that need longer battery life between charges. This is in addition to the fact that the more consumption there is, the hotter the product can get which limits performance noting the scheduling impact of designing and packaging that impacts cost as well. Mr. McAweeney said, "Chip designers are compelled to manage power!" Cadence Design Systems solution to this power management problem is to attack it on two fronts; leakage and dynamic power in collaboration with the Silicon Design Chain members referenced above. "Effective power management isn't really about one company trying to solve it and the customer gluing the pieces together, but rather a design chain collaborating together to solve the problem comprehensively," concluded McAweeney. *(Approved by Speaker)*

**Dennis Monticelli**  
National Fellow, National Semiconductor

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## KEYNOTE ADDRESS:

**John Bourgoin**  
CEO and President, MIPS Technologies  
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## CPU PANEL: Multiprocessor SoCs, The Next Hurdle for the IP Market

Moderator: John Mashey, Consultant, Techvisor

*How many CPUs per person are there in the U.S. today?*

"There are about 150 per person!"—Mr. Mashey

**Carl Schlachte**  
CEO, ARC International

[www.arc.com](http://www.arc.com)

According to Mr. Schlachte, there are four "P's" in the SoC industry that are critical to designers of consumer electronics devices: greater Product differentiation, protection from Piracy, lower Power consumption, and lower Price. "For too long CPU designers have been bound by fixed architectures that are unable to scale to meet the requirements of high-volume applications," commented Mr. Schlachte. "ARC's patented configurable technology marries standardization and customization in a way that offers a badly needed alternative to the cookie-cutter approach to SoC design. Today some of the world's largest semiconductor companies have standardized upon our configurable SoC technology and are shipping millions of ARC-Based products to markets globally." *(Approved by Speaker)*

**Mark Templeton**  
CSO and President, ARM, Inc.

[www.arm.com](http://www.arm.com)

Mr. Templeton pointed out the challenges designers face in their effort to reduce energy. The focus of the ARM11 MP Core addresses this issue by extending control over power usage by providing voltage and frequency scaling. This is in addition to powering down unused processors. "The tricky part of multi-processor integrations is coordination of interrupts and caches," said Mr. Templeton. ARM's solution provides an advanced multi-processor core that integrates as easily as a single CPU." He concluded his presentation with the concept of the smart phone of 2008. *(Approved by Speaker)*

**Grant Pierce**  
President and CEO, Sonics, Inc.

[www.sonicsinc.com](http://www.sonicsinc.com)

Mr. Pierce said there is a new and emerging IP market called the intelligent internal interconnect. "There has been a significant increase in data flow design complexity requiring a shift in design methodology to intelligent interconnects in order for companies to significantly reduce development times while also dramatically lowering SoC development costs," said Mr. Pierce. "Over 100 million Sonics enabled chips have been shipped and this new model promotes parallel tasks," concluded Mr. Pierce. *(Approved by Speaker)*

**Craig Lytle**  
Vice President, System Engineering, Altera Corp.

[www.altera.com](http://www.altera.com)

## **ANALOG IP PANEL: Is Portable Analog IP Possible, and if so – When?**

Moderator: Jim Feldhan, President, Semico Research Corp.

### **Guy Lemieux**

**President and CEO, LTRIM Technologies**

[www.ltrim.com](http://www.ltrim.com)

LTRIM Technologies is a pure analog IP provider specializing in power management and data conversion. The company has patented Laser Fine Tuning Technology which trims embedded resistors in the substrate. The reality of analog IP is the lower geometries are just as challenging as they are in digital. "There is limited analog engineering expertise, especially at SoC companies," commented Mr. Lemieux. "Furthermore, the challenges of analog design in CMOS include; threshold voltages, manufacturing process variations, noise, (maturity of) analog models at foundries and the slower evolution of available EDA tools." So what solutions are available? There is the development of circuit architectures that are less sensitive to transistor threshold voltages. There are optimized transistor matching techniques and advanced layout techniques for substrate noise attenuation. "My prediction is that within five years every SoC will contain analog IP to some degree and integration expertise will be the key—imagine analog in the heart of digital," concluded Mr. Lemieux. *(Approved by Speaker)*

### **John G. Maneatis, Ph.D.,**

**President, True Circuits, Inc.**

[www.truecircuits.com](http://www.truecircuits.com)

True Circuits is a leading supplier of analog/mixed signal IP with a significant focus on R&D to develop superior circuit technologies. Mr. Maneatis said, "The time for analog IP is now." He continued to promote the need for robust circuit technology. "Key features and performance must be an integral part of the design and these designs must have the features and flexibility to minimize customization steps," said Mr. Maneatis. "Much of True Circuits' design standardization is possible because of automation and this includes the design deliverables and user documentation." In summary, traditional user-intensive analog design techniques will not support the needs of successful analog IP companies of the future. "Their needs to be a focus on robust circuit technologies, design standardization, improved CAD tools and close foundry relationships," concluded Mr. Maneatis. *(Approved by Speaker)*

### **Sandipan Bhanot**

**CEO, Knowlent Corporation**

[www.knowlent.com](http://www.knowlent.com)

Knowlent is an EDA/IP company focused on electrical verification of interface designs. According to Mr. Bhanot, "The business case for analog IP and portability is clear and we must focus on the technical challenges of making portability possible." There are factors that aid in portability endeavors such as; operating at higher levels of abstraction, common test-benches and automatic translation across levels and ports. "The visible future includes common verification platforms that will get entrenched plus there will be a constant move towards higher levels of abstraction," concluded Mr. Bhanot. *(Approved by Speaker)*